Title (en)

PROGRAMMABLE PROCESSOR ARCHITECTURE

Title (de)

PROGRAMMIERBARE PROZESSORARCHITEKTUR

Title (fr)

ARCHITECTURE DE PROCESSEUR PROGRAMMABLE

Publication

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Application

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Priority

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- US 59841704 P 20040802

Abstract (en)

[origin: WO2006017339A2] One embodiment of the present includes a heterogenous, high-performance, scalable processor having at least one W-type sub-processor capable of processing W bits in parallel, W being an integer value, at least one N-type sub-processor capable of processing N bits in parallel, N being an integer value wherein and smaller than W by a factor of two. The processor further includes a shared bus coupling the at least one W-type sub-processor and at least one N-type subprocessor and memory shared coupled to the at least one W-type sub-processor and the at least one N-type sub-processor, wherein the W-type sub-processor rearranges memory to accommodate execution of applications allowing for fast operations.

IPC 8 full level

G06F 15/76 (2006.01)

CPC (source: EP KR)

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