

Title (en)  
PROGRAMMABLE PROCESSOR ARCHITECTURE

Title (de)  
PROGRAMMIERBARE PROZESSORARCHITEKTUR

Title (fr)  
ARCHITECTURE DE PROCESSEUR PROGRAMMABLE

Publication  
**EP 1779256 A4 20071128 (EN)**

Application  
**EP 05771043 A 20050712**

Priority  
• US 2005024867 W 20050712  
• US 58769104 P 20040713  
• US 59841704 P 20040802

Abstract (en)  
[origin: WO2006017339A2] One embodiment of the present includes a heterogenous, high-performance, scalable processor having at least one W-type sub-processor capable of processing W bits in parallel, W being an integer value, at least one N-type sub-processor capable of processing N bits in parallel, N being an integer value wherein and smaller than W by a factor of two. The processor further includes a shared bus coupling the at least one W-type sub-processor and at least one N-type subprocessor and memory shared coupled to the at least one W-type sub-processor and the at least one N-type sub-processor, wherein the W-type sub-processor rearranges memory to accommodate execution of applications allowing for fast operations.

IPC 8 full level  
**G06F 15/76** (2006.01)

CPC (source: EP KR)  
**G06F 9/3001** (2013.01 - EP); **G06F 9/30018** (2013.01 - EP); **G06F 9/30032** (2013.01 - EP); **G06F 9/3885** (2013.01 - EP);  
**G06F 15/00** (2013.01 - KR); **G06F 15/76** (2013.01 - KR); **G06F 15/7864** (2013.01 - EP)

Citation (search report)  
• [A] EP 1126368 A2 20010822 - TEXAS INSTRUMENTS INC [US]  
• [X] STOLBERG H-J ET AL: "HiBRID-SoC: a multi-core system-on-chip architecture for multimedia signal processing applications", DESIGN, AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION, 2003 MUNICH, GERMANY 3-7 MARCH 2003, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 3 March 2003 (2003-03-03), pages 8 - 13suppl, XP010673491, ISBN: 0-7695-1870-2  
• [A] HOOGENBOOM: "TASKING helps Siemens with 32-bit TriCore architecture design", INTERNET CITATION, November 1997 (1997-11-01), XP002259125, Retrieved from the Internet <URL:http://www.tasking.com/technology/tricore-archtecture.pdf> [retrieved on 20031024]  
• [A] MANI BHADRA VAYA: "VITURBO: A Reconfigurable Architecture for Ubiquitous Wireless Networks", THESIS: MASTER OF SCIENCE. ELECTRICAL AND COMPUTER ENGINEERING RICE UNIVERSITY HOUSTON, August 2002 (2002-08-01), pages complete, XP002314960  
• See references of WO 2006017339A2

Designated contracting state (EPC)  
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR

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**WO 2006017339 A2 20060216**; **WO 2006017339 A3 20060406**; CA 2572954 A1 20060216; EP 1779256 A2 20070502;  
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