Title (en)

CURRENT MIRROR ARRANGEMENT

Title (de)

STROMSPIEGELANORDNUNG

Title (fr)

SYSTEME DE MIROIR DE COURANT

Publication

EP 1784701 A1 20070516 (DE)

Application

EP 05790411 A 20050831

Priority

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- DE 102004042354 A 20040901

Abstract (en)

[origin: WO2006024525A1] The invention relates to a current mirror arrangement wherein two current mirror transistors (2, 3) form a current mirror. Two cascade transistors (11, 12) are interconnected with the two current mirror transistors (2, 3), forming a cascade stage. Said cascade transistors (11, 12) respectively comprise a plurality of partial transistors (13, 14, 15; 16, 17, 18) that are interconnected in series in terms of the controlled sections thereof. In this way, the connection nodes of the current mirror transistors can be connected to a connection node between two partial transistors (14, 15). This, in turn, causes an enlargement of the input voltage range for a current source (4) that supplies an input current for the current mirror.

IPC 8 full level

G05F 3/26 (2006.01)

CPC (source: EP US)

G05F 3/262 (2013.01 - EP US)

Citation (search report)

See references of WO 2006024525A1

Citation (examination)

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- YAN S.; SANCHEZ-SINENCIO E.: "Low voltage Analog Circuit Design Techniques: A Tutorial", IEICE TRANS. ANALOG INTEGRATED CIRCUITS AND SYSTEMS, vol. E00-A, no. 2, 2 February 2000 (2000-02-02), pages 1 - 17

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