Title (en)

GENERATING AN INTEGRATED CIRCUIT IDENTIFIER

Title (de)

ERZEUGUNG EINER KENNUNG EINER INTEGRIERTEN SCHALTUNG

Title (fr)

GENERATION D'UN IDENTIFIANT D'UN CIRCUIT INTEGRE

Publication

EP 1807869 A2 20070718 (FR)

Application

EP 05800239 A 20050923

Priority

- FR 2005050772 W 20050923
- FR 0452140 A 20040923

Abstract (en)

[origin: WO2006032823A2] The invention concerns the generation of a chip identifier (2) bearing at least one integrated circuit, which consists in providing a cutout of least one conductive path (4) by cutting the chip, the position of the cutting line (3) relative to the chip conditioning the identifier.

IPC 8 full level

H01L 23/544 (2006.01)

CPC (source: EP US)

H01L 23/544 (2013.01 - EP US); H01L 2223/5444 (2013.01 - EP US); H01L 2924/0002 (2013.01 - EP US)

C-Set (source: EP US)

H01L 2924/0002 + H01L 2924/00

Citation (search report)

See references of WO 2006032823A2

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

FR 2875623 A1 20060324; EP 1807869 A2 20070718; US 2008023854 A1 20080131; US 2011062601 A1 20110317; US 7871832 B2 20110118; US 8330158 B2 20121211; WO 2006032823 A2 20060330; WO 2006032823 A3 20061207

DOCDB simple family (application)

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