Title (en)

Device and method of adapting the potential of the substrate of an MOS transistor

Title (de)

Vorrichtung und Verfahren zur Anpassung des Potenzials des Substrats eines MOS-Transistors

Title (fr)

Dispositif et procédé d'adaptation du potentiel du substrat d'un transistor MOS

Publication

**EP 1835374 A1 20070919 (FR)**

Application

**EP 07104336 A 20070316**

Priority

FR 0650938 A 20060317

Abstract (en)

The circuit (30) has a casing enclosing a substrate (B) e.g. silicon on insulator (SOI), of a MOS power transistor (MSW) e.g. N-channel MOS power transistor, for ensuring an electric insulation of the substrate. A capacitor (C1) is connected to the substrate with a source (SP) that provides a source voltage (Vp) with two values during two periods, respectively, where one period is lower than half of the other period. An independent claim is also included for a method for biasing a substrate of a MOS transistor.

Abstract (fr)

L'invention concerne un circuit (30) de polarisation du substrat (B) d'un transistor MOS (MSW) comprenant un élément capacitif (C 1 ) reliant le substrat (B) du transistor MOS à une source (SP) d'une tension (V P ) alternative.

IPC 8 full level

**G05F 3/20** (2006.01)

CPC (source: EP US)

**G05F 3/205** (2013.01 - EP US)

Citation (applicant)

US 4491746 A 19850101 - KOIKE HIDEHARU [JP]

Citation (search report)

- [XA] US 4491746 A 19850101 - KOIKE HIDEHARU [JP]
- [A] US 5184030 A 19930202 - CHUNG JIN Y [KR], et al
- [A] US 5210446 A 19930511 - NIUYA TAKAYUKI [JP], et al
- [A] US 6175263 B1 20010116 - LEE KYU-CHAN [KR], et al

Designated contracting state (EPC)

DE FR GB IT

Designated extension state (EPC)

AL BA HR MK YU

DOCDB simple family (publication)

**EP 1835374 A1 20070919**; **EP 1835374 B1 20150722**; US 2007262809 A1 20071115; US 7622983 B2 20091124

DOCDB simple family (application)

**EP 07104336 A 20070316**; US 68704707 A 20070316