Title (en)

Processor and method of controlling the same

Title (de)

Prozessor und Steuerungsverfahren dafür

Title (fr)

Processeur et son procédé de commande

Publication

EP 1840735 A2 20071003 (EN)

Application

EP 07108697 A 20001215

Priority

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- JP 2000067789 A 20000310

Abstract (en)

A processor includes a history control unit (51) that stores a storage destination of a result obtained by executing a second instruction that is executed prior to a first instruction placed before the second instruction. When it is determined that the address of first data to be processed by the first instruction is included in the address region of second data to be processed by the second instruction, the history control unit (51) overwrites the result obtained by the execution of the first instruction on the second data corresponding to the address. The processor can perform a load operation prior to a store operation while avoiding ambiguous memory reference, and achieves high-speed operations.

IPC 8 full level

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CPC (source: EP KR US)

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