Title (en)

Method for manufacturing a semi-conductor element with a metal gate electrode assembled in a double trench structure

Title (de)

Verfahren zur Herstellung eines Halbleiterbauelements mit einer in einer Doppelgrabenstruktur angeordneten metallischen Gateelektrode

Title (fr)

Procédé de fabrication d'un élément semi-conducteur doté d'une électrode porte métallique agencée dans une double structure à tranchée

Publication

EP 1858064 A3 20080528 (DE)

Application

EP 07009105 A 20070505

Priority

DE 102006022507 A 20060515

Abstract (en)

[origin: EP1858064A2] Semiconductor component fabrication includes forming first opening that determines gate foot structure in auxiliary and intermediate layers, and transferring first opening into contact layer up to stop layer with narrow recess structure as first partial recess. The auxiliary layer is under-etched with broad recess structure. An opening is formed in the stop layer with first partial recess as mask. The partial recess in the contact layer is widened to form the broad recess. Gate metal (15) for gate foot and gate head is deposited into narrow recess and onto auxiliary layer, respectively. Semiconductor component fabrication includes depositing a semiconductor layer sequence for FET. The layer sequence includes channel layer, barrier layer, low-doped shielding layer, stop layer, and highly-doped contact layer. An intermediate layer and an auxiliary layer are deposited on the contact layer. A first opening that determines a structure of gate foot is formed in the auxiliary and intermediate layers and transferred into the contact layer up to the stop layer with a structure of narrow recess as a first partial recess. The auxiliary layer is under-etched with a structure of broad recess by selectively etching the intermediate layer. An opening is formed in the stop layer with the first partial recess as a mask. The partial recess in the contact layer is widened to form the broad recess, with the structure in the intermediate layer as a mask. The narrow recess in the shielding layer is exposed up to the barrier layer, with the opening in the stop layer. Gate metal for gate foot is deposited into the narrow recess, with the opening in the auxiliary layer as a mask, and gate metal for gate head is deposited onto the auxiliary layer.

IPC 8 full level

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CPC (source: EP US)

H01L 21/28587 (2013.01 - EP US); **H01L 29/42316** (2013.01 - EP US); **H01L 29/66462** (2013.01 - EP US); **H01L 29/7783** (2013.01 - EP US); **H01L 29/7786** (2013.01 - EP US)

Citation (search report)

- [Y] US 6180968 B1 20010130 - KASAHARA KENSUKE [JP], et al
- [DY] US 2004082158 A1 20040429 - WHELAN COLIN S [US], et al
- [A] US 5364816 A 19941115 - BOOS J BRAD [US], et al
- [A] WO 03067664 A1 20030814 - HITACHI LTD [JP], et al
- [A] DE 10117741 A1 20021017 - UNITED MONOLITHIC SEMICONDUCT [DE]

Designated contracting state (EPC)

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Designated extension state (EPC)

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DOCDB simple family (publication)

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DOCDB simple family (application)

EP 07009105 A 20070505; AT 07009105 T 20070505; DE 102006022507 A 20060515; DE 502007006073 T 20070505; US 80077007 A 20070507