Title (en)

METHOD AND APPARATUS FOR REDUCING SYSTEM INACTIVITY DURING TIME DATA FLOAT DELAY AND EXTERNAL MEMORY WRITE

Title (de)

VERFAHREN UND VORRICHTUNG ZUR VERRINGERUNG VON SYSTEMINAKTIVITÄT WÄHREND EINER ZEITDATEN-FLOAT-VERZÖGERUNG UND EINES EXTERNEN SPEICHERSCHREIBVORGANGS

Title (fr)

PROCEDE ET APPAREIL PERMETTANT DE REDUIRE L'INACTIVITE D'UN SYSTEME AU COURS DU RETARD FLOTTANT DE DONNEES ET DE L'ECRITURE MEMOIRE EXTERNE

Publication

EP 1866777 A4 20080326 (EN)

Application

EP 06727521 A 20060324

Priority

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- FR 0503089 A 20050330
- US 12810905 A 20050511

Abstract (en)

[origin: WO2006103563A2] The invention comprises a system for reducing inactive periods in an integrated circuit. The integrated circuit is coupled to an external peripheral by an external data bus. The integrated circuit has a processor coupled to an internal data bus. The system comprises the following. An external bus circuit is coupled to the internal and external data busses. The bus interface circuit is configured to receive read and write signals for data request data. In response, the bus interfaces circuit transmits a wait signal until data from the external peripheral is available on the internal data bus. The wait signal indicates that the external and internal data busses are not available for other purposes. After the processor has received or transmits the data, the bus interface circuit stops transmitting the wait signal and transmits a busy signal. The busy signal indicates that the internal data bus is available and the external data bus is not available for other purposes.

IPC 8 full level

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CPC (source: EP KR)

G06F 3/00 (2013.01 - KR); **G06F 13/00** (2013.01 - KR); **G06F 13/40** (2013.01 - KR); **G06F 13/405** (2013.01 - EP); **G06F 13/4243** (2013.01 - EP)

Citation (search report)

- [A] WO 0054165 A1 20000914 - ATMEL CORP [US]
- See references of WO 2006103563A2

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DOCDB simple family (publication)

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DOCDB simple family (application)

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