Title (en)

Process for manufacturing a semiconductor wafer having SOI-insulated wells and semiconductor wafer thereby manufactured

Title (de)

Verfahren zur Herstellung einer Halbleiterscheibe mit SOI-Isolierten Gräben und entsprechende Halbleiterscheibe

Title (fr)

Procédé de fabrication d'une plaquette semiconductrice ayant des puits SOI isolés et plaquette semiconductrice correpondante

Publication

EP 1881527 A1 20080123 (EN)

Application

EP 06425494 A 20060717

Priority

EP 06425494 A 20060717

Abstract (en)

A process for manufacturing a semiconductor wafer including SOI-insulation wells envisages forming, in a die region (5; 105) of a semiconductor body (2, 17; 102, 117), buried cavities (20, 21, 22; 110', 111', 112') and semiconductor structural elements (13', 14', 15'; 113', 114', 115'), which traverse the buried cavities and are distributed in the die region (5; 105). The process moreover includes the step of oxidizing selectively first adjacent semiconductor structural elements (13'; 113'), arranged inside a closed region (6; 106), and preventing oxidation of second semiconductor structural elements (14'; 114') outside the closed region (6; 106), so as to form a die buried dielectric layer (29; 129) selectively inside the closed region (6; 106).

IPC 8 full level

H01L 21/762 (2006.01)

CPC (source: EP US)

H01L 21/76264 (2013.01 - EP US); **H01L 21/7682** (2013.01 - US)

Citation (search report)

- [X] EP 1324382 A1 20030702 - ST MICROELECTRONICS SRL [IT]
- [XA] EP 1480266 A2 20041124 - ST MICROELECTRONICS SA [FR]
- [XA] EP 1073112 A1 20010131 - ST MICROELECTRONICS SRL [IT]

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DE FR GB IT

Designated extension state (EPC)

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DOCDB simple family (publication)

EP 1881527 A1 20080123; US 2008029817 A1 20080207; US 2011133186 A1 20110609; US 7906406 B2 20110315; US 9105690 B2 20150811

DOCDB simple family (application)

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