Title (en)

STORED-PROGRAM CONTROL

Title (de)

SPEICHERPROGRAMMIERBARE STEUERUNG

Title (fr)

DISPOSITIF DE COMMANDE A MEMOIRE PROGRAMMABLE

Publication

**EP 1894066 A1 20080305 (DE)**

Application

**EP 06754159 A 20060606**

Priority

- EP 2006005389 W 20060606
- AT 9622005 A 20050607

Abstract (en)

[origin: WO2006131317A1] Disclosed is a stored-program control comprising a CPU operating at a first clock frequency, a configurable logic circuit operating at a second clock frequency, and a bus to which the CPU and the logic circuit are connected. A control program encompassing a first task and a second task is stored in the stored-program control. The first task is stored in the stored-program control in such a way that the same can be executed by the CPU while the second task in configured in the logic circuit. The logic circuit is configured such that the second task (11) can be executed by the logic circuit in exactly one clock pulse of the logic circuit.

IPC 8 full level

**G05B 19/05** (2006.01)

CPC (source: EP)

**G05B 19/056** (2013.01); G05B 2219/13068 (2013.01); G05B 2219/13071 (2013.01); G05B 2219/15057 (2013.01)

Citation (search report)

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