

Title (en)

Resistive memory including bipolar transistor access devices

Title (de)

Resistiver Speicher mit Zugangsvorrichtungen für bipolare Transistoren

Title (fr)

Mémoire résistive dotée de dispositifs d'accès à transistor bipolaire

Publication

EP 1927991 B1 20140507 (EN)

Application

EP 07022409 A 20071119

Priority

US 60272006 A 20061121

Abstract (en)

[origin: EP1927991A2] A memory includes a first bipolar transistor, a first bit line, and a first resistive memory element coupled between a collector of the first bipolar transistor and the first bit line. The memory includes a second bit line, a second resistive memory element coupled between an emitter of the first bipolar transistor and the second bit line, and a word line coupled to a base of the first bipolar transistor.

IPC 8 full level

G11C 13/00 (2006.01); **H01L 27/24** (2006.01)

CPC (source: EP KR US)

G11C 11/5678 (2013.01 - EP US); **G11C 11/5685** (2013.01 - EP US); **G11C 13/0004** (2013.01 - EP US); **G11C 13/0007** (2013.01 - EP US); **G11C 13/02** (2013.01 - KR); **H10B 63/32** (2023.02 - EP US); **H10B 63/80** (2023.02 - EP US); **H10N 70/231** (2023.02 - EP US); **H10N 70/826** (2023.02 - EP US); **H10N 70/8828** (2023.02 - EP US); **H10N 70/884** (2023.02 - EP US); **G11C 2213/32** (2013.01 - EP US); **G11C 2213/79** (2013.01 - EP US); **Y10T 29/49002** (2015.01 - EP US)

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

EP 1927991 A2 20080604; **EP 1927991 A3 20090902**; **EP 1927991 B1 20140507**; CN 101188140 A 20080528; CN 101188140 B 20100721; JP 2008234813 A 20081002; KR 20080046123 A 20080526; US 2008117667 A1 20080522; US 7436695 B2 20081014

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EP 07022409 A 20071119; CN 200710187511 A 20071121; JP 2007300593 A 20071120; KR 20070119020 A 20071121; US 60272006 A 20061121