Title (en)

BINARY FREQUENCY DIVIDER

Title (de)

BINÄRER FREQUENZTEILER

Title (fr)

DIVISEUR DE FREQUENCE BINAIRE

Publication

EP 1964268 A1 20080903 (FR)

Application

EP 06841817 A 20061128

Priority

- FR 2006002604 W 20061128
- FR 0513121 A 20051222

Abstract (en)

[origin: FR2895601A1] The method involves defining a dividing set point (B2) and threshold values based on the set point. A counting value (VAL) is incremented in synchronization with a pulse edge of an input signal (CK1). The value is compared with the threshold values, and control signals (DET1, DET2) are produced. Control signals (SDET1, SDET2) shifted from a half-period of the input signal with respect to the signals (DET1, DET2) are produced. An output signal (CK2) is generated from the signals such that the period or duty factor of the signal (CK2) is adjusted equal to the half-period of the signal (CK1). Independent claims are also included for the following: (1) a binary frequency divider for receiving an input signal and providing an output signal (2) an integrated circuit comprising a binary frequency divider.

IPC 8 full level

H03K 23/66 (2006.01)

CPC (source: EP US)

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