

Title (en)

Circuit structure of high performance time-to-digital converter

Title (de)

Schaltungsstruktur für einen Hochleistungs-Zeit-Digital-Wandler

Title (fr)

Structure de circuit pour convertisseur temps-numérique haute performance

Publication

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Application

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Priority

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Abstract (en)

The invention discloses a circuit structure of a high performance time-to-digital converter including a delay link loop generating low bit data, a counter generating high bit data and a compensated control source. The delay link loop counts low bits and sends a thus-generated signal in a specific cycle to the counter. The counter accumulates a period of the signal in the specific cycle as high bits of the time-to-digital converter. The compensated control source compensates and controls a voltage signal of the delay link loop. The invention has the following advantages: a high measurement precision; a fast processing speed; the connection of the outputs of the latches with the high bit counter can ensure correctness of cycle and carry; the introduction of the compensated control source can ensure consistency of the system; and no high requirement is exerted on the components, and hence the circuit structure is easy to implement.

IPC 8 full level

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CPC (source: EP)

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Cited by

CN106302014A; CN113495816A; CN110266310A; CN114326908A; CN117555212A

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