Title (en)

Circuit structure of high performance time-to-digital converter

Title (de)

Schaltungsstruktur für einen Hochleistungs-Zeit-Digital-Wandler

Title (fr)

Structure de circuit pour convertisseur temps-numérique haute performance

Publication

EP 1971032 A3 20100203 (EN)

Application

EP 08102491 A 20080311

Priority

CN 200710037977 A 20070312

Abstract (en)

[origin: EP1971032A2] The invention discloses a circuit structure of a high performance time-to-digital converter including a delay link loop generating low bit data, a counter generating high bit data and a compensated control source The delay link loop counts low bits and sends a thus-generated signal in a specific cycle to the counter. The counter accumulates a period of the signal in the specific cycle as high bits of the time-to-digital converter. The compensated control source compensates and controls a voltage signal of the delay link loop. The invention has the following advantages: a high measurement precision; a fast processing speed; the connection of the outputs of the latches with the high bit counter can ensure correctness of cycle and carry; the introduction of the compensated control source can ensure consistency of the system; and no high requirement is exerted on the components, and hence the circuit structure is easy to implement.

IPC 8 full level

H03M 1/50 (2006.01)

CPC (source: EP)

G04F 10/005 (2013.01)

Citation (search report)

- [A] US 6348839 B1 20020219 - ARAMAKI YOSHINORI [JP]
- [A] US 5905412 A 19990518 - RASMUSSEN RICHARD R [US]
- [XI] HERVE C ET AL: "A 75ps rms time resolution BiCMOS time to digital converter optimized for high rate imaging detectors", NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - A:ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT, ELSEVIER, AMSTERDAM, NL, vol. 481, no. 1-3, 1 April 2002 (2002-04-01), pages 566 - 574, XP004347538, ISSN: 0168-9002
- [A] WATANABE T ET AL: "A CMOS TIME-TO-DIGITAL CONVERTER LSI WITH HALF-NANOSECOND RESOLUTION USING A RING GATE DELAY LINE", IEICE TRANSACTIONS ON ELECTRONICS, ELECTRONICS SOCIETY, TOKYO, JP, vol. E76-C, no. 12, 1 December 1993 (1993-12-01), pages 1774 - 1779, XP000426739, ISSN: 0916-8524

Cited by

CN106302014A; CN113495816A; CN110266310A; CN114326908A; CN117555212A

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

Designated extension state (EPC)

AL BA MK RS

DOCDB simple family (publication)

EP 1971032 A2 20080917; **EP 1971032 A3 20100203**; **EP 1971032 B1 20130619**; CN 100539428 C 20090909; CN 101043215 A 20070926

DOCDB simple family (application)

EP 08102491 A 20080311; CN 200710037977 A 20070312