

Title (en)

Circuit structure of high performance time-to-digital converter

Title (de)

Schaltungsstruktur für einen Hochleistungs-Zeit-Digital-Wandler

Title (fr)

Structure de circuit pour convertisseur temps-numérique haute performance

Publication

**EP 1971032 B1 20130619 (EN)**

Application

**EP 08102491 A 20080311**

Priority

CN 200710037977 A 20070312

Abstract (en)

[origin: EP1971032A2] The invention discloses a circuit structure of a high performance time-to-digital converter including a delay link loop generating low bit data, a counter generating high bit data and a compensated control source. The delay link loop counts low bits and sends a thus-generated signal in a specific cycle to the counter. The counter accumulates a period of the signal in the specific cycle as high bits of the time-to-digital converter. The compensated control source compensates and controls a voltage signal of the delay link loop. The invention has the following advantages: a high measurement precision; a fast processing speed; the connection of the outputs of the latches with the high bit counter can ensure correctness of cycle and carry; the introduction of the compensated control source can ensure consistency of the system; and no high requirement is exerted on the components, and hence the circuit structure is easy to implement.

IPC 8 full level

**G04F 10/00** (2006.01)

CPC (source: EP)

**G04F 10/005** (2013.01)

Citation (examination)

US 5331295 A 19940719 - JELINEK JULES J [US], et al

Cited by

CN113495816A; CN106302014A; CN110266310A; CN114326908A; CN117555212A

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