

Title (en)

EFFICIENT MEMORY HIERARCHY MANAGEMENT

Title (de)

EFFIZIENTE SPEICHERHIERARCHIEVERWALTUNG

Title (fr)

GESTION EFFICACE DE LA HIERARCHIE DES MEMOIRES

Publication

**EP 1974256 B1 20100505 (EN)**

Application

**EP 07710245 A 20070122**

Priority

- US 2007060815 W 20070122
- US 33628206 A 20060120

Abstract (en)

[origin: US2007174553A1] In a processor, there are situations where instructions and some parts of a program may reside in a data cache prior to execution of the program. Hardware and software techniques are provided for fetching an instruction in the data cache after having a miss in an instruction cache to improve the processor's performance. If an instruction is not present in the instruction cache, an instruction fetch address is sent as a data fetch address to the data cache. If there is valid data present in the data cache at the supplied instruction fetch address, the data actually is an instruction and the data cache entry is fetched and supplied as an instruction to the processor complex. An additional bit may be included in an instruction page table to indicate on a miss in the instruction cache that the data cache should be checked for the instruction.

IPC 8 full level

**G06F 9/38** (2006.01)

CPC (source: EP KR US)

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