Title (en)

PROCESS FOR FABRICATING A FIELD-EFFECT TRANSISTOR WITH SELF-ALIGNED GATES

Title (de)

VERFAHREN ZUR HERSTELLUNG EINES FELDEFFEKTTRANSISTORS MIT SELBSTJUSTIERTEN GATES

Title (fr)

PROCEDE DE REALISATION D'UN TRANSISTOR A EFFET DE CHAMP A GRILLES AUTO-ALIGNEES

Publication

EP 1999786 A2 20081210 (FR)

Application

EP 07731203 A 20070326

Priority

- FR 2007000520 W 20070326
- FR 0602682 A 20060328

Abstract (en)

[origin: WO2007110507A2] A first gate, formed on a substrate, is surmounted by a hard layer (11), intended, with first spacers (13) surrounding the first gate, to act as an etching mask for defining the channel (2a) and a pad that defines a space used subsequently to form a gate cavity (22). The hard layer is preferably made of silicon nitride. Before inverting and bonding, a defining layer (17), preferably made of amorphous silicon or of polysilicon, is formed in order to define drain and source zones. After inversion and bonding of the assembly to a second substrate (20), a second gate is formed in the gate cavity (22). Next, the defining layer (17) is at least partially silicided before the metal source and drain electrodes are produced.

IPC 8 full level

H01L 21/336 (2006.01); **H01L 21/84** (2006.01); **H01L 29/786** (2006.01)

CPC (source: EP US)

H01L 29/458 (2013.01 - EP US); **H01L 29/66772** (2013.01 - EP US); **H01L 29/78648** (2013.01 - EP US); **H01L 29/78654** (2013.01 - EP US); H01L 27/1266 (2013.01 - EP US); H01L 29/66553 (2013.01 - EP US); H01L 29/78684 (2013.01 - EP US)

Citation (search report)

See references of WO 2007110507A2

Designated contracting state (EPC)

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DOCDB simple family (publication)

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