

Title (en)
Wiring substrate

Title (de)
Verdrahtungssubstrat

Title (fr)
Substrat de câblage

Publication
EP 2006911 A3 20110803 (EN)

Application
EP 08158268 A 20080613

Priority
JP 2007165464 A 20070622

Abstract (en)
[origin: EP2006911A2] There is provided a wiring substrate 10. The wiring substrate includes: a semiconductor substrate 16 having a through hole 26; an insulating film 17, 18, 19 provided to cover an upper surface 16A, a lower surface 16B and a first surface of the semiconductor substrate 16, the first surface corresponding to a side surface of the through hole 26; a through electrode 21 provided in the through hole 26; a first wiring pattern 23 disposed on an upper surface side of the semiconductor substrate 16 and coupled to the through electrode 21; and a second wiring pattern 24 disposed on a lower surface side of the semiconductor substrate 16 and coupled to the through electrode 21. A first air gap 32 is provided between the first wiring pattern 23 and the insulating film 17 formed on the upper surface, and a second air gap 33 is provided between the second wiring pattern 24 and the insulating film 18 formed on the lower surface.

IPC 8 full level
H01L 23/498 (2006.01); **H01L 23/14** (2006.01)

CPC (source: EP US)
H01L 23/147 (2013.01 - EP US); **H01L 23/49827** (2013.01 - EP US); **H01L 2224/16225** (2013.01 - EP US); **H01L 2224/16227** (2013.01 - EP US); **H01L 2924/15311** (2013.01 - EP US)

Citation (search report)

- [A] EP 1612860 A2 20060104 - SHINKO ELECTRIC IND CO [JP]
- [A] US 6265312 B1 20010724 - SIDHWA ARDESHIR JEHangIR [US], et al
- [A] US 6806570 B1 20041019 - LEE JIN-YUAN [TW], et al

Designated contracting state (EPC)
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

Designated extension state (EPC)
AL BA MK RS

DOCDB simple family (publication)
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DOCDB simple family (application)
EP 08158268 A 20080613; JP 2007165464 A 20070622; US 14203908 A 20080619