Title (en)

ETCHED NANOFIN TRANSISTORS

Title (de)

GEÄTZTE NANOFIN-TRANSISTOREN

Title (fr)

TRANSISTORS À NERVURES DE TAILLE NANOMÉTRIQUE GRAVÉES

Publication

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Application

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- US 39740606 A 20060404

Abstract (en)

[origin: WO2007114927A1] One aspect of the present subject matter relates to a method for forming a transistor. According to an embodiment, a fin is formed from a crystalline substrate. A first source/drain region is formed in the substrate beneath the fin. A surrounding gate insulator is formed around the fin. A surrounding gate is formed around the fin and separated from the fin by the surrounding gate insulator. A second source/drain region is formed in a top portion of the fin. Various embodiments etch a hole in a layer over the substrate, form sidewall spacers in the hole, form a fin pattern from the sidewall spacers, and etch into the crystalline substrate to form the fin from the substrate using a mask corresponding to the fin pattern. Other aspects are provided herein.

IPC 8 full level

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Citation (examination)

- US 2003006410 A1 20030109 - DOYLE BRIAN [US]
- US 6063688 A 20000516 - DOYLE BRIAN S [US], et al
- See also references of WO 2007114927A1

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