

Title (en)

POWER HOUSING FOR SEMICONDUCTOR CHIPS AND THE ARRANGEMENT THEREOF FOR HEAT DISSIPATION

Title (de)

LEISTUNGSGEHÄUSE FÜR HALBLEITERCHIPS UND DEREN ANORDNUNG ZUR WÄRMEABFUHR

Title (fr)

BOÎTIER DE PUISSANCE POUR PUCES À SEMI-CONDUCTEUR ET CONFIGURATION DUDIT BOÎTIER POUR LA DISSIPATION DE CHALEUR

Publication

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Application

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Abstract (en)

[origin: WO2007045112A1] The invention relates to a surface-mountable power housing (1) for semiconductor chips (10) and the arrangement thereof for heat dissipation at cooling media (15) in high-power components by reducing the constructionally dictated thermal resistances lying in series. The power housing is formed in such a way that the underside can be connected directly to the heat sink (15) through an opening (21) in the wiring plane (25), and the required wiring plane is not incorporated. The housing is embodied from a chip carrier substrate (12) and a housing carrier substrate (13), which are provided with electrical connections for contact-connecting the semiconductor chips (10) to the wiring plane (25). The power housing preferably comprises ceramic materials or silicon.

IPC 8 full level

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