Title (en)
SCALABLE MEMORY SYSTEM

Title (de)
SKALIERBARES SPEICHERSYSTEM

Title (fr)
SYSTÈME DE MÉMOIRE ÉVOLUTIF

Publication
EP 2062261 A1 20090527 (EN)

Application
EP 07800496 A 20070822

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• CA 2007001469 W 20070822
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• US 86877306 P 20061206
• US 90200307 P 20070216
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Abstract (en)
[origin: WO2008022454A1] A memory system architecture has serially connected memory devices. The memory system is scalable to include any number of memory devices without any performance degradation or complex redesign. Each memory device has a serial input/output interface for communicating between other memory devices and a memory controller. The memory controller issues commands in at least one bitstream, where the bitstream follows a modular command protocol. The command includes an operation code with optional address information and a device address, so that only the addressed memory device acts upon the command. Separate data output strobe and command input strobe signals are provided in parallel with each output data stream and input command data stream, respectively, for identifying the type of data and the length of the data. The modular command protocol is used for executing concurrent operations in each memory device to further improve performance.

IPC 8 full level
G11C 8/18 (2006.01); **G06F 12/00** (2006.01); **G06F 13/16** (2006.01); **G06F 13/40** (2006.01); **G11C 7/10** (2006.01); **G11C 7/20** (2006.01); **G11C 8/04** (2006.01); **G11C 8/06** (2006.01); **G11C 11/34** (2006.01); **G11C 16/02** (2006.01)

CPC (source: EP KR)
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Designated extension state (EPC)
AL BA HR MK RS

DOCDB simple family (publication)
WO 2008022454 A1 20080228; CA 2659828 A1 20080228; CN 101506895 A 20090812; CN 101506895 B 20120627; CN 102760476 A 20121031; EP 2062261 A1 20090527; EP 2062261 A4 20100106; JP 2010501916 A 20100121; JP 2012226786 A 20121115; JP 5575474 B2 20140820; KR 101476463 B1 20141224; KR 101476515 B1 20141224; KR 20090045366 A 20090507; KR 20120110157 A 20121009; TW 200828338 A 20080701; TW I437577 B 20140511

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