

Title (en)

ARRAY OF NON-VOLATILE MEMORY CELLS WITH FLOATING GATES FORMED OF SPACERS IN SUBSTRATE TRENCHES

Title (de)

ANORDNUNG NICHTFLÜCHTIGER SPEICHERZELLEN MIT AUS ABSTANDHALTERN IN SUBSTRATGRÄBEN GEFORMTEN SCHWEBENDEN GATES

Title (fr)

MATRICE DE CELLULES DE MÉMOIRE NON VOLATILE À GRILLES FLOTTANTES À CONFIGURATION D'ESPACEURS DANS DES TRANCHÉES DE SUBSTRAT

Publication

EP 2064733 A2 20090603 (EN)

Application

EP 07842450 A 20070913

Priority

- US 2007078420 W 20070913
- US 53331306 A 20060919
- US 53331706 A 20060919

Abstract (en)

[origin: WO2008036552A2] In order to reduce the integrated circuit area that is occupied by an array of a given number of flash memory cells, floating gate charge storage elements are positioned along sidewalls of substrate trenches, preferably being formed of doped polysilicon spacers. An array of dual floating gate memory cells includes cells with this structure, as an example. A NAND array of memory cells is another example of an application of this cell structure. The memory cell and array structures have wide application to various specific NOR and NAND memory cell array architectures.

IPC 8 full level

H01L 21/28 (2006.01); **H01L 21/8247** (2006.01); **H01L 29/423** (2006.01); **H10B 69/00** (2023.01)

CPC (source: EP KR)

H01L 29/40114 (2019.08 - EP); **H01L 29/42336** (2013.01 - EP KR); **H01L 29/66825** (2013.01 - KR); **H01L 29/7881** (2013.01 - EP KR); **H10B 41/27** (2023.02 - EP KR); **H10B 41/35** (2023.02 - EP); **H10B 69/00** (2023.02 - EP)

Citation (examination)

- US 5973356 A 19991026 - NOBLE WENDELL P [US], et al
- US 5616510 A 19970401 - WONG CHUN C D [US]

Designated contracting state (EPC)

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Designated extension state (EPC)

AL BA HR MK RS

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