

Title (en)

A MULTI-TRANSISTOR BASED NON-VOLATILE MEMORY CELL WITH DUAL THRESHOLD VOLTAGE

Title (de)

NICHT FLÜCHTIGE SPEICHERZELLE MIT DOPPELSCHWELLENSPANNUNG AUF BASIS MEHRERER TRANSISTOREN

Title (fr)

CELLULE DE MÉMOIRE NON VOLATILE À PLUSIEURS TRANSISTORS DOTÉE D'UNE TENSION DE SEUIL DOUBLE

Publication

EP 2074649 A2 20090701 (EN)

Application

EP 07826550 A 20070926

Priority

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Abstract (en)

[origin: WO2008038236A2] A multi-transistor based non- volatile memory cell M1 arranged on a semiconductor substrate 1 includes at least one access transistor AT1; AT2; AT2'; AT2" and at least one memory transistor TM2a; TM2b; TM2c; TM2d. The at least one access transistor is a "normally-off " transistor and includes first and second diffusion regions S1, S2, an access channel region R1, and an access gate AG. The access channel region is intermediate the first and second diffusion regions. The at least one memory transistor includes third and fourth diffusion regions S2, S3, a channel region R2, a charge trapping element O1-N-O2 and a control gate CG. The channel region is intermediate the third and fourth diffusion regions, and the charge trapping element is above the channel region with the control gate being arranged above the charge trapping element. The semiconductor substrate is of a first conductivity type. The at least one memory transistor is provided with a memory threshold voltage window with an upper limit above and a lower limit below zero Volt.

IPC 8 full level

H01L 21/336 (2006.01); **G11C 16/04** (2006.01); **H01L 21/28** (2006.01); **H01L 21/8247** (2006.01); **H01L 27/115** (2006.01); **H01L 29/788** (2006.01); **H01L 29/792** (2006.01)

CPC (source: EP)

H01L 29/66833 (2013.01); **H01L 29/792** (2013.01); **H10B 43/30** (2023.02); **H10B 69/00** (2023.02); **G11C 16/0466** (2013.01); **H01L 29/40114** (2019.07); **H01L 29/40117** (2019.07); **H01L 29/66825** (2013.01); **H01L 29/7881** (2013.01); **H10B 41/35** (2023.02)

Citation (search report)

See references of WO 2008038236A2

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