Title (en)
   CONCURRENT READING OF STATUS REGISTERS

Title (de)
   GLEICHZEITIGE LESUNG VON STATUSREGISTERN

Title (fr)
   LECTURE DE REGISTRE D'ÉTAT CONCURRENT

Publication
   EP 2076905 B1 20101208 (EN)

Application
   EP 07844009 A 20071009

Priority
   • US 2007080779 W 20071009
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Abstract (en)
   [origin: WO2008045856A2] Status information comprising data not stored in a memory array is efficiently read from a plurality of parallel memory devices sharing an N-bit data bus by configuring each memory device to drive the status information on a different subset M of the N bits, and tri-state the remaining N-M bits. Each memory device is additionally configured to drive zero, one or more data strobes associated with the subset M, and tri-state the remaining data strobes. A memory controller may simultaneously read status information from two or more memory devices in parallel, with each memory device driving a separate subset M of the N-bit bus. Each memory device may serialize the status information, and drive it on the subset M of the bus in burst form. Each memory device may include a configuration register initialized by a memory controller to define its subset M.

IPC 8 full level
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