

Title (en)

Process and temperature compensation in CMOS circuits

Title (de)

Verfahren und Temperatenausgleich in CMOS-Schaltungen

Title (fr)

Processus et compensation de température dans des circuits CMOS

Publication

**EP 2124125 A1 20091125 (EN)**

Application

**EP 08156699 A 20080521**

Priority

EP 08156699 A 20080521

Abstract (en)

A circuit arrangement using CMOS technology is described comprising at least a first circuit (10,20) and a second, compensation circuit (50) for adaptively generating a biasing parameter ( $V_{bias}$ ) for counter-acting temperature and process variations in the first circuit (10,20). The second circuit (50) is based on a constant- $g_m$  bias generator and comprises a NMOS transistor (NM R ) operating in ohmic region. The second circuit (50) comprises two stages (51,52) with a substantially identical structure.

IPC 8 full level

**G05F 3/26** (2006.01)

CPC (source: EP)

**G05F 3/26** (2013.01)

Citation (search report)

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US9959915B2; WO2017099926A1

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

Designated extension state (EPC)

AL BA MK RS

DOCDB simple family (publication)

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