

Title (en)
LEVEL SHIFTER CIRCUIT INCORPORATING TRANSISTOR SNAP-BACK PROTECTION

Title (de)
PEGELUMSETZERSCHALTUNG MIT TRANSISTOR-EINSCHNAPPSCHUTZ

Title (fr)
CIRCUIT DE DÉCALAGE DE NIVEAU INCORPORANT UNE PROTECTION DE RETRAIT DE TRANSISTOR

Publication
EP 2132873 A4 20100602 (EN)

Application
EP 08744804 A 20080331

Priority
• US 2008058933 W 20080331
• US 69501107 A 20070331
• US 69501307 A 20070331

Abstract (en)
[origin: WO2008121977A2] Level shift circuits are disclosed for level shifting an input signal corresponding to a first voltage domain, to generate a pair of complementary output signals corresponding to a second, higher-voltage domain. Snap-back sensitive devices in a discharge circuit for a high voltage output node are protected, irrespective of the loading on the output node, and without requiring precise transistor sizing as a function of the output loading. The snap-back sensitive devices are protected by a voltage shifter circuit in series with the sensitive devices, to limit the voltage across the sensitive devices, even for a high capacitance output node at its highest output voltage. The voltage shifter circuit is then bypassed to provide for an output low level that fully reaches the lower power supply rail.

IPC 8 full level
H03K 19/0185 (2006.01); **H03K 17/10** (2006.01); **H03K 19/017** (2006.01)

CPC (source: EP KR)
H03K 3/35613 (2013.01 - EP); **H03K 17/102** (2013.01 - EP); **H03K 19/01721** (2013.01 - EP); **H03K 19/0185** (2013.01 - KR)

Citation (search report)
• [I] US 2002175737 A1 20021128 - DEBATY PASCAL [FR]
• [A] US 2002079545 A1 20020627 - DRAY CYRILLE [FR], et al
• [A] RWANG-CHERNG CHOW ET AL: "New voltage level shifting circuits for low power CMOS interface applications", IEEE INTERNATIONAL MIDWEST SYMPOSIUM,, vol. 1, 25 July 2004 (2004-07-25), pages 1_533 - 1_536, XP010739027, ISBN: 978-0-7803-8346-3
• [A] LIM J-H ET AL: "A NOVEL HIGH-SPEED AND LOW-VOLTAGE CMOS LEVEL-UP/DOWN SHIFTER DESIGN FOR MULTIPLE-POWER AND MULTIPLE-CLOCK DOMAIN CHIPS", IEICE TRANSACTIONS ON ELECTRONICS, ELECTRONICS SOCIETY, TOKYO, JP LNKD- DOI:10.1093/IETELE/E90-C.3.644, vol. E90C, no. 3, 1 March 2007 (2007-03-01), pages 644 - 648, XP001541508, ISSN: 0916-8524
• [A] TRAN C Q ET AL: "Low-power high-speed level shifter design for block-level dynamic voltage scaling environment", INTEGRATED CIRCUIT DESIGN AND TECHNOLOGY, 2005. ICICDT 2005. 2005 INTERNATIONAL CONFERENCE ON AUSTIN, TX, USA MAY 9-11, 2005, PISCATAWAY, NJ, USA, IEEE LNKD- DOI:10.1109/ICICDT.2005.1502637, 9 May 2005 (2005-05-09), pages 229 - 232, XP010832287, ISBN: 978-0-7803-9081-2
• See references of WO 2008121977A2

Cited by
CN109347473A; CN108667450A

Designated contracting state (EPC)
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

DOCDB simple family (publication)
WO 2008121977 A2 20081009; WO 2008121977 A3 20081204; CN 101682328 A 20100324; CN 101682328 B 20140430;
EP 2132873 A2 20091216; EP 2132873 A4 20100602; EP 2132873 B1 20120822; JP 2010524303 A 20100715; JP 4926275 B2 20120509;
KR 101505396 B1 20150325; KR 20100016050 A 20100212; TW 200847627 A 20081201; TW I350055 B 20111001

DOCDB simple family (application)
US 2008058933 W 20080331; CN 200880018315 A 20080331; EP 08744804 A 20080331; JP 2010501285 A 20080331;
KR 20097022680 A 20080331; TW 97111717 A 20080331