

Title (en)

IMPROVEMENTS RELATING TO SIMD PARALLEL PROCESSORS

Title (de)

VERBESSERUNGEN IM BEZUG AUF SIMD-PARALLELPROZESSOREN

Title (fr)

PERFECTIONNEMENTS PORTANT SUR DES PROCESSEURS PARALLÈLES SIMD

Publication

**EP 2140367 A1 20100106 (EN)**

Application

**EP 08718975 A 20080402**

Priority

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Abstract (en)

[origin: WO2008120001A1] A processing element of a Single Instruction Multiple Data parallel processing array processor is described where the processing element is configured to implement two bits at-a-time arithmetic operations local to the processing element. The processing element comprises: a plurality of operand registers arranged to store operands and results for arithmetic operations; an arithmetic logic unit for effecting the two bits at-a-time logical arithmetic operations including a Booth's algorithm mathematical operation, where subgroups of a multiplier are used to determine multiples (summands) of an operand to be summed together to determine the multiplication result; and variation means for enabling local conditional variation of the mathematical operation; the variation means comprising a Booth's algorithm delay register which provides the least significant bit of a current multiplier subgroup, the register being arranged to read the most significant bit of the current subgroup and to use this as the least significant bit of the next subgroup for the next summand determination operation.

IPC 8 full level

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CPC (source: EP)

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Citation (search report)

See references of WO 2008120001A1

Citation (examination)

BEHROOZ PARHAMI: "Computer Arithmetic Algorithms and Hardware Designs - excerpt Chapter 10", 31 December 2000 (2000-12-31), NEW YORK, pages 157 - 161, ISBN: 978-0-19-512583-2, [retrieved on 20130506]

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