Title (en)

HIGH-FREQUENCY RECEIVER WITH MULTIPLE-CHANNEL DIGITAL PROCESSING

Title (de)

HOCHFREQUENZEMPFÄNGER MIT DIGITALER MEHRKANALVERARBEITUNG

Title (fr)

RÉCEPTEUR HAUTE FRÉQUENCE À TRAITEMENT NUMÉRIQUE MULTI-CANAUX

Publication

EP 2145387 A2 20100120 (FR)

Application

EP 08787934 A 20080410

Priority

- FR 2008000499 W 20080410
- FR 0702668 A 20070412

Abstract (en)

[origin: WO2008142278A2] In the receive subsystem, the analogue-digital converter (40) works on the output of the low-noise amplifier (33), at a chosen rate (F), which corresponds to a bandwidth sampling. The processing stages comprise a custom circuit (5), with * an input memory (510) arranged to contain N successive digital samples, renewed at the chosen rate in blocks of M samples, * a complex digital low-pass filtering function (511, 512), of chosen cut-off frequency, operating on the input memory to supply N filtered digital samples (515), * an M-periodic summing function (531) on the N filtered digital samples, supplying M filtered and summed digital samples (533), * an M ´ M discrete Fourier transform stage (55), operating on these M filtered and summed digital samples, the digital signals on the M outputs (559) of the Fourier transform representing M separate channels, of width defined by the cut-off frequency of the abovementioned low-pass filter.

IPC 8 full level

H03H 17/02 (2006.01); **G01S 7/285** (2006.01); **G01S 13/00** (2006.01); **H03H 17/06** (2006.01)

CPC (source: EP US)

G01S 7/352 (2013.01 - EP US); **G01S 7/356** (2021.05 - EP); **G01S 7/358** (2021.05 - EP); **G01S 13/003** (2013.01 - EP US); **H03H 17/0685** (2013.01 - EP US); G01S 7/356 (2021.05 - US); G01S 7/358 (2021.05 - US); H03H 2017/0214 (2013.01 - EP US); H03H 2218/06 (2013.01 - EP US)

Citation (search report)

See references of WO 2008142278A2

Citation (examination)

- GIL SAVIR: "MSc Thesis: Scalable and Reconfigurable Digital Front-End for SDR Wideband Channelizer", 1 September 2011 (2011-09-01), DELFT, NL, XP055020395, Retrieved from the Internet <URL:http://ce.et.tudelft.nl/publicationfiles/1206_716_Gil_Savir-MSc_thesis.pdf> [retrieved on 20120227]
- "Envelope Detector", 6 December 2012 (2012-12-06), XP055046994, Retrieved from the Internet <URL:http://en.wikipedia.org/w/index.php?title=Envelope_detector&oldid=494565578> [retrieved on 20121206]
- "Multirate Digital Signal Processing", 21 March 1981, PRENTICE-HALL, ISBN: 978-0-13-605162-6, article RONALD E. CROCHIERE ET AL: "section 7.2 - Uniform DFT Filter Banks and Short-time Fourier Analyzers and Synthesizers", pages: 296 - 327, XP055046101

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

Designated extension state (EPC)

AL BA MK RS

DOCDB simple family (publication)

FR 2915038 A1 20081017; **FR 2915038 B1 20120803**; CN 101702958 A 20100505; CN 101702958 B 20131016; EP 2145387 A2 20100120; JP 2010527169 A 20100805; JP 5269876 B2 20130821; US 2010178894 A1 20100715; US 8428532 B2 20130423; WO 2008142278 A2 20081127; WO 2008142278 A3 20090115

DOCDB simple family (application)

FR 0702668 A 20070412; CN 200880011780 A 20080410; EP 08787934 A 20080410; FR 2008000499 W 20080410; JP 2010502547 A 20080410; US 45077308 A 20080410