Title (en)

MEMORY POINT OF STATIC MEMORY AND APPLICATION FOR AN IMAGE SENSOR

Title (de)

SPEICHERPUNKT EINES STATISCHEN SPEICHERS UND ANWENDUNG FÜR EINEN BILDSENSOR

Title (fr)

POINT MEMOIRE DE MEMOIRE STATIQUE ET APPLICATION A UN CAPTEUR D'IMAGE

Publication

EP 2188810 A2 20100526 (FR)

Application

EP 08804079 A 20080912

Priority

- EP 2008062114 W 20080912
- FR 0706463 A 20070914

Abstract (en)

[origin: WO2009034156A2] The invention relates to a memory point for an SRAM-type memory (static memory). The memory point traditionally comprises two inverters (INV, INVB) mounted head-to-tail between two nodes (N and NB), and at least one access transistor (TS) that can be made conductive during a writing phase and connected between a first node (N) and a line of data to be written (DL, DLW), characterised in that it comprises an isolation transistor (TAB) serially inserted between the output of a first inverter (INVB) and a first node (N), the isolation transistor (TAB) being controlled by an isolation signal at the beginning of a writing phase. The power consumption is reduced when the state of the memory point must be inverted. The invention can be used in an image sensor having numerous in-line pixels.

IPC 8 full level

G11C 11/417 (2006.01); **G11C 11/419** (2006.01)

CPC (source: EP US)

G11C 11/412 (2013.01 - EP US)

Citation (search report)

See references of WO 2009034156A2

Citation (examination)

ALY R E ET AL: "Novel 7T sram cell for low power cache design", SOC CONFERENCE, 2005. PROCEEDINGS. IEEE INTERNATIONAL HERNDON, VA, USA 25-28 SEPT. 2005, PISCATAWAY, NJ, USA,IEEE LNKD- DOI:10.1109/SOCC.2005.1554488, 25 September 2005 (2005-09-25), pages 171 - 174, XP010861192, ISBN: 978-0-7803-9264-9

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