Title (en)

Method for etching 3d structures in a semiconductor substrate, including surface preparation

Title (de)

Verfahren zum Ätzen von 3-D-Strukturen in ein Halbleitersubstrat, einschließlich der Oberflächenbehandlung

Title (fr)

Procédé de gravure de structures en 3D dans un substrat à semi-conducteur, incluant la préparation des surfaces

Publication

EP 2224469 A2 20100901 (EN)

Application

EP 10154439 A 20100223

Priority

US 15542609 P 20090225

Abstract (en)

The present invention is related to method for producing 3D structures in a semiconductor substrate using Deep Reactive Ion Etching (DRIE), comprising at least the steps of: - providing a substrate (1), and then - grinding the backside of the substrate in order to achieve a thinned substrate, wherein extrusions (2) and native oxides (3) are left after said grinding step, and then - performing a surface treatment selected from the group consisting of a wet etching step and a dry etching step in order to remove at least said native oxides (3) and extrusions (2) on the surface of said backside of the substrate which are causes for the grass formation during subsequent etching, and then - performing deep reactive ion etching in order to achieve 3D vias.

IPC 8 full level

H01L 21/304 (2006.01); **H01L 21/3065** (2006.01)

CPC (source: EP US)

H01L 21/02057 (2013.01 - EP US); **H01L 21/304** (2013.01 - EP US); **H01L 21/3065** (2013.01 - EP US)

Citation (applicant)

- US 5501893 A 19960326 - LAERMER FRANZ [DE], et al
- B. SCHWARTZ; H. ROBBINS, J. ELECTROCHEM. SOC., vol. 123, 1976, pages 1903

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US9006703B2

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

Designated extension state (EPC)

AL BA RS

DOCDB simple family (publication)

EP 2224469 A2 20100901; **EP 2224469 A3 20150325**; US 2010216308 A1 20100826

DOCDB simple family (application)

EP 10154439 A 20100223; US 71154410 A 20100224