Title (en)

SRAM MEMORY CELL BASED ON DOUBLE-GATE TRANSISTORS, PROVIDED WITH MEANS FOR IMPROVING THE WRITE MARGIN

Title (de)

SRAM-SPEICHERZELLE AUF BASIS VON DOPPELGATE-TRANSISTOREN MIT MITTEL ZUR ERWEITERUNG EINES SCHREIBBEREICHS

Title (fr)

CELLULE MÉMOIRE SRAM À TRANSISTORS DOUBLE GRILLE DOTEE DE MOYENS POUR AMELIORER LA MARGE EN ECRITURE

Publication

EP 2245632 A1 20101103 (FR)

Application

EP 09712534 A 20090216

Priority

- EP 2009051819 W 20090216
- FR 0851027 A 20080218

Abstract (en)

[origin: WO2009103687A1] Random-access memory cell, comprising: two double-gate access transistors (TA3L, TA3R) placed, respectively, between a first bit line (BLL) and a first storage node (L) and between a second bit line (BLR) and a second storage node (R); a word line (WL); a first double-gate charge transistor (TL1L) and a second double-gate charge transistor (TL1R); a first double-gate conduction transistor (TD1L) and a second double-gate conduction transistor (TD1R), the cell comprising: means for applying a given potential Vcell to at least one electrode of each of the charge or conduction transistors; and means for varying said given potential Vcell.

IPC 8 full level

G11C 11/412 (2006.01); **G11C 11/419** (2006.01)

CPC (source: EP US)

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Designated contracting state (EPC)

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Designated extension state (EPC)

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DOCDB simple family (publication)

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