

Title (en)

DESIGN SIMULATION USING PARALLEL PROCESSORS

Title (de)

DESIGNSIMULATION ANHAND PARALLELER PROZESSOREN

Title (fr)

SIMULATION DE CONCEPTION UTILISANT DES PROCESSEURS PARALLÈLES

Publication

EP 2257874 A2 20101208 (EN)

Application

EP 09724182 A 20090325

Priority

- IL 2009000330 W 20090325
- US 3981708 P 20080327
- US 7946108 P 20080710
- US 8680308 P 20080807
- US 11067608 P 20081103

Abstract (en)

[origin: WO2009118731A2] A method for design simulation includes partitioning a verification task of a design (100) into a first plurality of atomic Processing Elements (PEs - 108) having execution dependencies (112), each execution dependency specifying that a respective first PE is to be executed before a respective second PE. The method further includes computing an order for executing the PEs on a multiprocessor device (32), which includes a second plurality of processors (44) operating in parallel and schedules the PEs for execution by the processors according to a built-in scheduling policy. The order induces concurrent execution of the PEs by different ones of the processors without violating the execution dependencies, irrespective of the scheduling policy. The PEs are executed on the processors in accordance with the computed order and the scheduling policy, to produce a simulation result. A performance of the design is verified responsive to the simulation result.

IPC 8 full level

G06F 17/50 (2006.01); **G06F 9/45** (2006.01)

CPC (source: EP US)

G06F 8/45 (2013.01 - EP US); **G06F 30/327** (2020.01 - US); **G06F 30/33** (2020.01 - EP US); **G06F 30/3308** (2020.01 - US)

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