

Title (en)

Process for manufacturing an integrated device with "damascene" field insulation

Title (de)

Herstellungsverfahren für ein integriertes Bauelement mit "damaszener" Feldisolation

Title (fr)

Procédé de fabrication d'un circuit intégré avec isolation de champ de type "damasquinage"

Publication

EP 2306509 A1 20110406 (EN)

Application

EP 10182571 A 20100929

Priority

IT TO20090738 A 20090929

Abstract (en)

An integrated device includes a semiconductor body (11), in which an STI insulation structure (15) is formed, which delimits laterally first active areas (17) and at least one second active area (18), respectively, in a low-voltage region (12) and in a power region (13) of the semiconductor body (11). The integrated device moreover includes low-voltage CMOS components (50, 51), accommodated in the first active areas (17), and a power component (52) in the second active area (18). The power component (52) has a source region (45), a body region (32), a drain-contact region (46), and at least one field-insulating region (27), set between the body region (32) and the drain-contact region (46). The field-insulating region (27) is provided entirely on the semiconductor body (11).

IPC 8 full level

H01L 21/8238 (2006.01); **H01L 21/336** (2006.01); **H01L 27/092** (2006.01); **H01L 29/423** (2006.01); **H01L 29/74** (2006.01)

CPC (source: EP US)

H01L 21/823807 (2013.01 - EP US); **H01L 21/823878** (2013.01 - EP US); **H01L 27/0922** (2013.01 - EP US); **H01L 29/42368** (2013.01 - EP US); **H01L 29/66681** (2013.01 - EP US); **H01L 29/7816** (2013.01 - EP US)

Citation (search report)

- [Y] WO 2006052791 A2 20060518 - TEXAS INSTRUMENTS INC [US], et al
- [Y] US 2005199951 A1 20050915 - SHIMIZU AKIRA [JP], et al
- [Y] US 2008006875 A1 20080110 - OHTSUKA MASAYA [JP], et al
- [Y] US 2006138584 A1 20060629 - KO KWANG Y [KR]
- [Y] US 2006086992 A1 20060427 - KANG MI-HYUN [KR], et al
- [Y] US 6339001 B1 20020115 - BRONNER GARY B [US], et al
- [A] US 2006148110 A1 20060706 - SUNG WOONG J [KR]
- [A] KIM J ET AL: "p</E1>-channel LDMOS transistor using new tapered field oxidation technology", ELECTRONICS LETTERS, IEE STEVENAGE, GB LNKD- DOI:10.1049/EL:19981303, vol. 34, no. 19, 17 September 1998 (1998-09-17), pages 1893 - 1894, XP006010337, ISSN: 0013-5194

Designated contracting state (EPC)

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