

Title (en)

A NAND BASED NMOS NOR FLASH MEMORY CELL/ARRAY AND A METHOD OF FORMING SAME

Title (de)

AUF NAND BASIERENDE NMOS-NOR-FLASH-SPEICHERZELLE/-MATRIX UND HERSTELLUNGSVERFAHREN DAFÜR

Title (fr)

RÉSEAU/CELLULE DE MÉMOIRE FLASH NON-OU MOS À CANAL N À BASE DE NON-ET SON PROCÉDÉ DE FORMATION

Publication

EP 2308051 A1 20110413 (EN)

Application

EP 09743052 A 20090507

Priority

- US 2009002817 W 20090507
- US 12685408 P 20080507

Abstract (en)

[origin: WO2009137065A1] A NOR flash nonvolatile memory device provides the memory cell size and a low current program process of a NAND flash nonvolatile memory device and the fast, asynchronous random access of a NOR flash nonvolatile memory device. The NOR flash nonvolatile memory device has an array of NOR flash nonvolatile memory circuits. Each NOR flash nonvolatile memory circuit includes a plurality of charge retaining transistors serially connected in a NAND string. A drain of a topmost charge retaining transistor is connected to a bit line associated with the serially connected charge retaining transistors and a source of a bottommost charge retaining transistor is connected to a source line associated with the charge retaining transistors. Each control gate of the charge retaining transistors on each row is commonly connected to a word line. The charge retaining transistors are programmed and erased with a Fowler- Nordheim tunneling process.

IPC 8 full level

G11C 16/04 (2006.01)

CPC (source: EP)

G11C 11/5642 (2013.01); **G11C 16/0483** (2013.01); **G11C 16/08** (2013.01); **H10B 41/10** (2023.02); **H10B 41/30** (2023.02); **G11C 16/0433** (2013.01)

Citation (search report)

See references of WO 2009137065A1

Designated contracting state (EPC)

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Designated extension state (EPC)

AL BA RS

DOCDB simple family (publication)

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