

Title (en)

APPARATUS FOR TESTING INTEGRATED CIRCUITRY

Title (de)

VORRICHTUNG ZUM PRÜFEN VON INTEGRIERTEN SCHALTKREISEN

Title (fr)

APPAREIL DE TEST DE CIRCUITS INTÉGRÉS

Publication

EP 2326963 A4 20140122 (EN)

Application

EP 08782943 A 20080819

Priority

AU 2008001195 W 20080819

Abstract (en)

[origin: WO2010019981A1] A testing apparatus for testing integrated circuits mounted in a carrier includes a support assembly. A controller is mounted in the support assembly. The controller is programmed to process test signals from the integrated circuits. A retaining assembly is arranged on the support assembly and is configured to receive and retain the carrier during testing. A displacement mechanism is arranged on the support assembly for displacing the retaining assembly relative to the support assembly into and out of an operative condition. Testing circuitry is operatively connected to the controller and has at least test signal generation and measurement circuitry and adaptor circuitry for operative engagement with the integrated circuits being tested, the adaptor circuitry being configured to provide both a physical and an electrical interface with the integrated circuits.

IPC 8 full level

G01R 31/28 (2006.01); **B41J 2/01** (2006.01); **B41J 2/045** (2006.01); **G01R 1/02** (2006.01); **H01L 21/66** (2006.01)

CPC (source: EP KR)

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Citation (search report)

- [X1] US 7151388 B2 20061219 - GOPAL BALLSON [US], et al
- [X1] US 5227717 A 19930713 - TSURISHIMA KAZUYUKI [JP], et al
- [A] WO 2008053929 A1 20080508 - TOKYO ELECTRON LTD [JP], et al
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CN110441553A

Designated contracting state (EPC)

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