Title (en)

SERIAL-CONNECTED MEMORY SYSTEM WITH OUTPUT DELAY ADJUSTMENT

Title (de)

SERIELL GESCHALTETES SPEICHERSYSTEM MIT AUSGABEVERZÖGERUNGSEINSTELLUNG

Title (fr)

SYSTÈME DE MÉMOIRE CONNECTÉ EN SÉRIE PRÉSENTANT UN AJUSTEMENT DE DÉLAI DE SORTIE

Publication

EP 2329496 A4 20120613 (EN)

Application

EP 09817125 A 20090917

Priority

- CA 2009001271 W 20090917
- US 24196008 A 20080930
- US 24183208 A 20080930

Abstract (en)

[origin: WO2010037205A1] Systems and methods for correcting clock duty cycle and/or performing output delay adjustment are provided for application in serial- connected devices operating as slave devices. A master device provides a clock to the first slave device. Each slave device passes the clock to the next slave device in turn. The last slave device returns the clock to the master device. The master device compares the outgoing and returned clocks and determines if a duty cycle correction and/or an output delay adjustment is needed. If so, the master device generates and outputs commands for slave devices to perform duty cycle and/or output delay adjustment. The slave devices each have a circuit for performing duty cycle correction and/or output delay adjustment. In some implementations, each slave device is a memory device, and the master device is a memory controller.

IPC 8 full level

G11C 7/22 (2006.01); **G06F 13/42** (2006.01); **G11C 16/32** (2006.01)

CPC (source: EP KR)

G11C 7/1066 (2013.01 - EP); **G11C 7/1069** (2013.01 - EP); **G11C 7/22** (2013.01 - EP KR); **G11C 7/222** (2013.01 - EP); **G11C 16/32** (2013.01 - EP KR)

Citation (search report)

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- [XA] US 2006136618 A1 20060622 - GOWER KEVIN C [US], et al
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- See also references of WO 2010037205A1

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

DOCDB simple family (publication)

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