Title (en)

DATA SAMPLING CIRCUIT AND METHOD FOR CLOCK AND DATA RECOVERY

Title (de)

DATENABTASTSCHALTUNG UND VERFAHREN ZUR TAKT- UND DATENWIEDERGEWINNUNG

Title (fr)

CIRCUIT D'ÉCHANTILLONNAGE DE DONNÉES ET PROCÉDÉ DE RÉCUPÉRATION D'HORLOGE ET DE DONNÉES

Publication

EP 2335374 A1 20110622 (EN)

Application

EP 08877195 A 20081002

Priority

US 2008011416 W 20081002

Abstract (en)

[origin: WO2010039108A1] A clock and data recovery circuit and method are used in a digital data communications system. The circuit and method are effectively employed for high speed, burst-mode transmission and allow rapid recovery of the clock and data signals without the need for an extended header, and notwithstanding the presence of substantial timing jitter. The method adaptively selects from among three delay times for the extraction of data by identifying a frequently recurring incoming pattern in the incoming data. The delay time is selected in a manner that insures that the same pattern is present in the reconstructed, resynchronized output data.

IPC 8 full level

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H03L 7/06 (2013.01); **H03L 7/0805** (2013.01); **H04L 7/0338** (2013.01)

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