

Title (en)

METHOD AND APPARATUS FOR DITHERING IN MULTI-BIT SIGMA-DELTA DIGITAL-TO-ANALOG CONVERTERS

Title (de)

METHODE UND GERÄT ZUM DITHERN IN MULTI-BIT SIGMA DELTA DIGITAL ANALOG WANDLERN

Title (fr)

PROCÉDÉ ET APPAREIL DE TREMBLOTEMENT DANS DES CONVERTISSEURS NUMÉRIQUES À ANALOGIQUES SIGMA-DELTA À MULTIPLES BITS

Publication

EP 2351228 B1 20170118 (EN)

Application

EP 09741547 A 20091022

Priority

- US 2009061599 W 20091022
- US 10782008 P 20081023
- US 57189209 A 20091001

Abstract (en)

[origin: US2010103003A1] A multi-bit (M-bit, $M > 1$) or multi-level (nlev levels, $nlev > 2$, encoded on M bits where $M = \text{Floor}(\log_2(nlev))$) sigma-delta analog-to-digital converter (ADC) with a variable resolution multi-bit quantizer having its resolution (number of distinct output levels) and associated quantization thresholds changed for each voltage sample with a random or pseudo-random sequence N(n) to provide automatic dynamic dithering for removing undesired idle tones in the digital output of the sigma-delta ADC. The random integer numbers N(n) between 2 and nlev may be provided by a random or pseudo-random sequence generator, e.g., Galois linear feedback shift register in combination with digital comparators and an adder.

IPC 8 full level

H03M 3/04 (2006.01)

CPC (source: EP KR US)

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US 2004160348 A1 20040819 - HOCHSCHILD JAMES R [US]

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