

Title (en)

METHOD AND APPARATUS FOR IMPROVING POWER AND LOSS FOR INTERCONNECT CONFIGURATIONS

Title (de)

VERFAHREN UND VORRICHTUNG FÜR ERHÖHTE LEISTUNG UND GERINGEREN VERLUST IN VERNETZUNGSKONFIGURATIONEN

Title (fr)

PROCÉDÉ ET APPAREIL POUR AMÉLIORER LA PUISSANCE ET LA PERTE POUR DES CONFIGURATIONS D'INTERCONNEXION

Publication

EP 2428105 A4 20130529 (EN)

Application

EP 10772351 A 20100108

Priority

- US 2010000043 W 20100108
- US 21536909 P 20090504

Abstract (en)

[origin: WO2010129002A1] The present disclosure relates to embedding a power modification component such as a capacitance or a resistance inside of pads that are located to extend over and beyond the vias of the PCB so that a portion of the pad containing the embedded capacitance or resistance is located beyond where the vias or blinds are located. Each of the pads will include an opening that is located over a given one of the vias or blinds to permit that via to conduct through the opening. In this way the capacitance and the resistance will have a closer contact point the electrical component.

IPC 8 full level

H05K 1/18 (2006.01); **H05K 3/30** (2006.01)

CPC (source: EP KR)

H05K 1/023 (2013.01 - EP); **H05K 1/18** (2013.01 - KR); **H05K 1/185** (2013.01 - EP); **H05K 3/30** (2013.01 - KR); **H05K 1/0231** (2013.01 - EP); **H05K 1/0234** (2013.01 - EP); **H05K 1/112** (2013.01 - EP); **H05K 3/4046** (2013.01 - EP); **H05K 2201/096** (2013.01 - EP); **H05K 2201/10636** (2013.01 - EP); **Y02P 70/50** (2015.11 - EP)

Citation (search report)

- [X] EP 1098368 A1 20010509 - MATSUSHITA ELECTRIC IND CO LTD [JP]
- [X] US 2008013295 A1 20080117 - KURAMITSU KOUICHI [JP], et al
- [X] JP H11103170 A 19990413 - KYOCERA CORP
- See references of WO 2010129002A1

Designated contracting state (EPC)

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DOCDB simple family (application)

US 2010000043 W 20100108; CN 201080019789 A 20100108; EP 10772351 A 20100108; JP 2012509780 A 20100108; KR 20117025869 A 20100108; SG 2012005781 A 20100108