Title (en)

Cache memory apparatus, cache control method, and microprocessor system

Title (de)

Cachespeichervorrichtung, Cachesteuerverfahren und Mikroprozessorsystem

Title (fr)

Appareil de mémoire cache, procédé de commande de mémoire cache et système de microprocesseur

Publication

EP 2590082 A1 20130508 (EN)

Application

EP 12190816 A 20121031

Priority

JP 2011240780 A 20111102

Abstract (en)

A cache memory apparatus according to the present invention includes a cache memory that caches an instruction code corresponding to a fetch address and a cache control circuit that controls the instruction code to be cached in the cache memory. The cache control circuit caches an instruction code corresponding to a subroutine when the fetch address indicates a branch into the subroutine and disables the instruction code to be cached when the number of the instruction codes to be cached exceeds a previously set maximum number.

IPC 8 full level

G06F 9/38 (2006.01); **G06F 12/08** (2006.01)

CPC (source: EP US)

G06F 9/3804 (2013.01 - EP US); **G06F 12/0875** (2013.01 - EP US); **G06F 12/0888** (2013.01 - EP US)

Citation (applicant)

JP H09305490 A 19971128 - NEC CORP

Citation (search report)

- [YA] EP 0457403 A2 19911121 - KONINKL PHILIPS ELECTRONICS NV [NL]
- [YA] EP 1785876 A1 20070516 - HITACHI LTD [JP]
- [A] US 5687349 A 19971111 - MCGARITY RALPH C [US]

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

EP 2590082 A1 20130508; **EP 2590082 B1 20180117**; CN 103092773 A 20130508; CN 103092773 B 20171020; JP 2013097638 A 20130520; JP 5793061 B2 20151014; US 2013111140 A1 20130502; US 9317438 B2 20160419

DOCDB simple family (application)

EP 12190816 A 20121031; CN 201210432095 A 20121102; JP 2011240780 A 20111102; US 201213668009 A 20121102