

Title (en)

METHOD AND APPARATUS FOR CHECKING A MAIN MEMORY OF A PROCESSOR

Title (de)

VERFAHREN UND VORRICHTUNG ZUM PRÜFEN EINES HAUPTSPEICHERS EINES PROZESSORS

Title (fr)

PROCÉDÉ ET DISPOSITIF POUR VÉRIFIER LA MÉMOIRE PRINCIPALE D'UN PROCESSEUR

Publication

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Application

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Abstract (en)

[origin: WO2012007295A1] The invention relates to a method and an apparatus for checking a main memory (3) of a processor (1), comprising a cache memory (2) and a plurality of registers (R). According to the invention, before carrying out a memory test (T), a boot-up sequence which may be running at that time is interrupted, temporary data required for the memory test (T) is written to at least one register (6) and is held there, and the access from the cache memory (2) to the main memory (3) is activated. In this case, the access to the main memory (3) is carried out via the cache memory (2, 5) such that bit patterns (BM) are written to the cache memory (2, 5) and, via this, to the main memory (3), and are read out again from the main memory (3) via the cache memory (2) and are compared, wherein that area of the main memory (3) to be tested is larger than the size of the cache memory (2), and the boot-up sequence which was possibly interrupted before carrying out the memory test (T) is restarted or continued once the memory test (T) has been completed.

IPC 8 full level

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