

Title (en)
METHOD AND APPARATUS FOR TOKEN TRIGGERED MULTITHREADING

Title (de)
VERFAHREN UND VORRICHTUNG FÜR DURCH TOKEN AUSGELÖSTES MULTITHREADING

Title (fr)
PROCÉDÉ ET APPAREIL POUR MULTIFILIÈRE DÉCLENCHÉE PAR UN JETON

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Application
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Abstract (en)
[origin: US2004073781A1] Techniques for token triggered multithreading in a multithreaded processor are disclosed. An instruction issuance sequence for a plurality of threads of the multithreaded processor is controlled by associating with each of the threads at least one register which stores a value identifying a next thread to be permitted to issue one or more instructions, and utilizing the stored value to control the instruction issuance sequence. For example, each of a plurality of hardware thread units of the multithreaded processor may include a corresponding local register updatable by that hardware thread unit, with the local register for a given one of the hardware thread units storing a value identifying the next thread to be permitted to issue one or more instructions after the given hardware thread unit has issued one or more instructions. A global register arrangement may also or alternatively be used. The processor may be configured so as to permit the instruction issuance sequence to correspond to an arbitrary alternating even-odd sequence of threads, without introducing blocking conditions leading to thread stalls.

IPC 8 full level
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