Title (en)

Method of producing a high-voltage LDMOS transistor

Title (de)

Verfahren zur Herstellung eines Hochspannungs-LDMOS-Transistors

Title (fr)

Procédé de fabrication d'un transistor LDMOS haute tension

Publication

EP 2665101 B1 20181031 (EN)

Application

EP 12167851 A 20120514

Priority

EP 12167851 A 20120514

Abstract (en)

[origin: EP2665101A1] A first well (2) of a first type of conductivity is formed in a substrate (1). A second well (3) of an opposite type of conductivity is formed in the first well. A source region (4) is formed in the first well outside the second well. A drain region (5) is formed in the second well, leaving a drift region (13) in the second well between the drain region and the source region. A bulk contact region (6) is formed in the first well. A gate dielectric (8) and a gate electrode (9) are arranged on the substrate between the second well and the source region. The doping of the second well is reduced in the drift region by using an implantation mask (10) with a patterned window (11) comprising openings (12) that are confined in directions both along the drift region and transverse to the drift region.

IPC 8 full level

H01L 29/78 (2006.01); **H01L 21/336** (2006.01); **H01L 29/08** (2006.01); H01L 21/266 (2006.01); H01L 29/423 (2006.01)

CPC (source: EP US)

H01L 29/0847 (2013.01 - EP); **H01L 29/0878** (2013.01 - EP US); **H01L 29/66659** (2013.01 - EP); **H01L 29/7835** (2013.01 - EP); H01L 21/266 (2013.01 - EP); H01L 29/42368 (2013.01 - EP)

Cited by

WO2018040864A1

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

DOCDB simple family (publication)

EP 2665101 A1 20131120; **EP 2665101 B1 20181031**; WO 2013171012 A1 20131121

DOCDB simple family (application)

EP 12167851 A 20120514; EP 2013057828 W 20130415