Title (en)

PARALLELIZATION OF ERROR ANALYSIS CIRCUITRY FOR REDUCED POWER CONSUMPTION

Title (de)

PARALLELISIERUNG VON FEHLERANALYSESCHALTUNGEN FÜR VERMINDERTEN STROMVERBRAUCH

Title (fr)

PARALLÉLISATION DE CIRCUIT D'ANALYSE D'ERREURS POUR UNE CONSOMMATION D'ÉNERGIE RÉDUITE

Publication

EP 2689332 B1 20170104 (EN)

Application

EP 11719637 A 20110324

Priority

IB 2011000635 W 20110324

Abstract (en)

[origin: US2012246526A1] A memory device (e.g., a flash memory device) includes power efficient codeword error analysis circuitry. The circuitry analyzes codewords stored in the memory of the memory device to locate and correct errors in the codewords before the codewords are communicated to a host device that requests the codewords from the memory device. The circuitry includes a highly parallel configuration with reduced complexity (e.g., reduced gate count) that a controller may cause to perform the error analysis under most circumstances. The circuitry also includes an analysis section of greater complexity with a less parallel configuration that the controller may cause to perform the error analysis less frequently. Because the more complex analysis section runs less frequently, the error analysis circuitry may provide significant power consumption savings in comparison to prior designs for error analysis circuitry.

IPC 8 full level

G06F 11/10 (2006.01)

CPC (source: EP KR US)

G06F 11/1048 (2013.01 - EP KR US); **G11C 29/42** (2013.01 - KR); **H03M 13/1545** (2013.01 - EP KR US); **H03M 13/3707** (2013.01 - EP KR US); **H03M 13/6561** (2013.01 - EP KR US)

Designated contracting state (EPC)

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DOCDB simple family (publication)

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US 201113340286 A 20111229; CN 201180070667 A 20110324; EP 11719637 A 20110324; IB 2011000635 W 20110324; KR 20137025841 A 20110324; TW 101110236 A 20120323