

## Title (en)

PIXEL ARRAY AREA OPTIMIZATION USING STACKING SCHEME FOR HYBRID IMAGE SENSOR WITH MINIMAL VERTICAL INTERCONNECTS

## Title (de)

PIXELARRAY-BEREICHSOPTIMIERUNG DURCH EIN STAPELUNGSSCHEMA FÜR EINEN HYBRIDBILDSSENSOR MIT MINIMALEN SENKRECHTEN VERBINDUNGEN

## Title (fr)

OPTIMISATION DE ZONE DE MATRICE DE PIXELS À L'AIDE D'UN SCHÉMA D'EMPLIAGE POUR UN CAPTEUR D'IMAGES HYBRIDE COMPORTANT DES INTERCONNEXIONS VERTICALES MINIMALES

## Publication

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## Application

**EP 12782963 A 20120514**

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## Abstract (en)

[origin: WO2012155142A1] Embodiments of a hybrid imaging sensor that optimizes a pixel array area on a substrate using a stacking scheme for placement of related circuitry with minimal vertical interconnects between stacked substrates and associated features are disclosed. Embodiments of maximized pixel array size die size (area optimization) are disclosed, and an optimized imaging sensor providing improved image quality, improved functionality, and improved form factors for specific applications common to the industry of digital imaging are also disclosed. Embodiments of the above may include systems, methods and processes for staggering ADC or column circuit bumps in a column or sub-column hybrid image sensor using vertical interconnects are also disclosed.

## IPC 8 full level

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## C-Set (source: US)

**H01L 2924/0002 + H01L 2924/00**

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- [XY] EP 2234387 A1 20100929 - SONY CORP [JP]
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- See also references of WO 2012155142A1

## Designated contracting state (EPC)

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