

Title (en)

APPARATUS FOR GLITCHLESS CLOCK DIVIDER WITH FAST CLOCK CHANGE AND METHOD THEREOF

Title (de)

VORRICHTUNG FÜR STÖRUNGSFREIEN TAKTTEILER MIT SCHNELLER TAKTVERÄNDERUNG UND VERFAHREN DAFÜR

Title (fr)

APPAREIL POUR DIVISEUR D'HORLOGE SANS DÉFORMATION AVEC CHANGEMENT D'HORLOGE RAPIDE, ET PROCÉDÉ ASSOCIÉ

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Application

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Abstract (en)

[origin: WO2012168533A1] An apparatus comprising a clock shaper (510) configured to derive a frequency of a reference clock signal (501) into a plurality of n frequencies associated to a plurality of n gated clocks, Clock 0, Clock 1,..., Clock n-1 (571-0, 571-1,..., 571-n-1), and configured to generate a plurality of m clock enable signals (511-1, 511-2, 511-3, 511-4,..., 511-m), where n is a number of the gated clocks and m corresponds to a divisor; a plurality of n coupled clock selection and gating units (550-0, 550-1,..., 550-n-1) receiving the reference clock (501) and the plurality of m clock enable signals (511-1, 511-2, 511-3, 511-4,..., 511-m), and configured to select one of the plurality of m clock enable signals (511-1, 511-2, 511-3, 511-4,..., 511-m) and to gate to an output clock (571-0, 571-1,..., 571-n-1); and a phase decoding unit (530) configured to decode the plurality of m clock enable signals (511-1, 511-2, 511-3, 511-4,..., 511-m) based on a plurality of received division value per clock signals, and configured to generate a plurality of n clock selection signals (531-0, 531-1,..., 531-n-1), wherein one of the plurality of n clock selection signals (531-0, 531-1 531 -n-1) corresponds to a selected frequency of one of the plurality of frequencies of the plurality of n gated clocks (571-1, 571-2,..., 571-n-1); wherein the plurality of n coupled clock selection and gating units (550-0, 550-1 550-n-1) are responsive to the plurality of n clock selection signals (531-0, 531-1 531 -n-1) to generate the output clock (571-0, 571-1,..., 571 -n-1) with the selected frequency.

IPC 8 full level

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