

Title (en)

WAFER STRUCTURE FOR ELECTRONIC INTEGRATED CIRCUIT MANUFACTURING

Title (de)

WAFERSTRUKTUR ZUR HERSTELLUNG EINER ELEKTRONISCHEN INTEGRIERTEN SCHALTUNG

Title (fr)

STRUCTURE DE TRANCHE POUR LA FABRICATION DE CIRCUITS INTÉGRÉS ÉLECTRONIQUES

Publication

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Application

EP 12826159 A 20120824

Priority

- US 201113218308 A 20110825
- US 201113218273 A 20110825
- US 201113218335 A 20110825
- US 201113218345 A 20110825
- US 201113218352 A 20110825
- US 201113218292 A 20110825
- US 2012052293 W 20120824

Abstract (en)

[origin: WO2013028973A1] A bonded wafer structure having a handle wafer, a device wafer, and an interface region with an abrupt transition between the conductivity profile of the device wafer and the handle wafer is used for making semiconductor devices. The improved doping profile of the bonded wafer structure is well suited for use in the manufacture of integrated circuits. The bonded wafer structure is especially suited for making radiation-hardened integrated circuits.

IPC 8 full level

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Citation (search report)

- [X] EP 0327316 A2 19890809 - TOSHIBA KK [JP]
- [X] US 4935386 A 19900619 - NAKAGAWA AKIO [JP], et al
- [X] EP 0889509 A2 1990107 - HARRIS CORP [US]
- [X] CHING-FA YEH ET AL: "THE NOVEL PREPARATION OF P-N JUNCTION MESA DIODES BY SILICON-WAFER DIRECT BONDING (SDB)", JAPANESE JOURNAL OF APPLIED PHYSICS, JAPAN SOCIETY OF APPLIED PHYSICS, JP, vol. 31, no. 5A, 1 May 1992 (1992-05-01), pages 1535 - 1540, XP000355403, ISSN: 0021-4922, DOI: 10.1143/JJAP.31.1535
- See references of WO 2013028983A1

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