Title (en)

A TAMPER DETECTION ARRANGEMENT

Title (de)

MANIPULATIONSERKENNUNGSANORDNUNG

Title (fr)

SYSTÈME DE DÉTECTION D'ALTÉRATION

Publication

EP 2766929 A1 20140820 (EN)

Application

EP 12850746 A 20121029

Priority

IB 2012003115 W 20121029

Abstract (en)

[origin: WO2014068361A1] A tamper detection arrangement for use within an integrated circuit (1), the arrangement comprising: at least one input capacitor (4) having a first capacitance value; a feedback capacitor (5) having a second capacitance value; a sensing arrangement comprising an amplifier circuit having the at least one input capacitor as an input and the at least one feedback capacitor in a feedback loop across the amplifier operable to detect a change in the capacitance values between the at least one input capacitor and the feedback capacitor; and a protective shield to protect a sensitive area (2) of the integrated circuit from tampering, the shield being provided by the at least one input capacitor (4).

IPC 8 full level

H01L 23/58 (2006.01)

CPC (source: EP US)

G06F 21/60 (2013.01 - US); **G06F 21/87** (2013.01 - EP US); **H01L 23/576** (2013.01 - EP US); H01L 2924/0002 (2013.01 - EP US)

Citation (search report)

See references of WO 2014068361A1

Cited by

CN109782154A

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

WO 2014068361 A1 20140508; EP 2766929 A1 20140820; US 2014320151 A1 20141030; US 9514308 B2 20161206

DOCDB simple family (application)

IB 2012003115 W 20121029; EP 12850746 A 20121029; US 201414204739 A 20140311