

Title (en)  
TECHNIQUES FOR TILING ARRAYS OF PIXEL ELEMENTS

Title (de)  
VERFAHREN ZUR KACHELUNG VON PIXELELEMENTANORDNUNGEN

Title (fr)  
TECHNIQUES DE JUXTAPOSITION DE MATRICES D'ÉLÉMENTS DE PIXELS

Publication  
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Application  
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Abstract (en)  
[origin: WO2013059757A1] Sub-arrays such as tiles or chips (110; 410; 510; 610) having pixel elements (112; 212; 412; 512; 612; 712; 812; 912) arranged on a routing layer (150; 350) or carrier to form a larger array (100). Through-chip vias (128) or the like to the backside of the chip are used for connecting with the pixel elements. Edge features (204, 206, 208) of the tiles may provide for physical alignment, mechanical attachment and chip-to-chip communication. Edge damage tolerance with minimal loss of function may be achieved by moving unit cell circuitry (422; 522; 622) and the electrically active portions (FIGs. 7A,B,C; FIG. 8, FIGs. 9, 9A) of a pixel element away from the tile edge(s) while leaving the optically active portion closer to the edge(s) if minor damage will not cause a complete failure of the pixel. The pixel elements may be thermal emitter elements for IR image projectors, thermal detector elements for microbolometers, LED-based emitters, or quantum photon detectors such as those found in visible, infrared and ultraviolet FPAs (focal plane arrays), and the like. Various architectures (FIGs. 3A,B,C) are disclosed.

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