Title (en)

STACKED SEMICONDUCTOR DIE ASSEMBLIES WITH MULTIPLE THERMAL PATHS AND ASSOCIATED SYSTEMS AND METHODS

Title (de)

ANORDNUNGEN GESTAPELTER HALBLEITERCHIPS MIT EINER VIELZAHL AN WÄRMEPFADEN SOWIE SYSTEME UND VERFAHREN DAMIT

Title (fr)

ENSEMBLES DE PUCES SEMI-CONDUCTRICES EMPILÉES PRÉSENTANT PLUSIEURS TRAJETS THERMIQUES, ET SYSTÈMES ET PROCÉDÉS ASSOCIÉS

Publication

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Application

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Abstract (en)

[origin: US2013119527A1] A semiconductor die assembly comprises a plurality of semiconductor dice in a stack. Another semiconductor die is adjacent to the stack and has a region, which may comprise a relatively higher power density region, extends peripherally beyond the stack. Conductive elements extend between and electrically interconnect integrated circuits of semiconductor dice in the stack and of the other semiconductor die. Thermal pillars are interposed between semiconductor dice of the stack, and a heat dissipation structure, such as a lid, is in contact with an uppermost die of the stack and the high power density region of the other semiconductor die. Other die assemblies, semiconductor devices and methods of managing heat transfer within a semiconductor die assembly are also disclosed.

IPC 8 full level

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CPC (source: EP KR US)

H01L 23/34 (2013.01 - KR); **H01L 23/36** (2013.01 - EP US); **H01L 23/367** (2013.01 - KR); **H01L 23/3675** (2013.01 - US); **H01L 23/3677** (2013.01 - EP US); **H01L 23/3736** (2013.01 - EP US); **H01L 23/42** (2013.01 - EP US); **H01L 25/0657** (2013.01 - EP US); **H01L 25/18** (2013.01 - EP US); **H01L 25/50** (2013.01 - US); H01L 2224/16145 (2013.01 - EP US); H01L 2224/16227 (2013.01 - EP US); H01L 2224/17181 (2013.01 - EP US); H01L 2224/73204 (2013.01 - EP US); H01L 2225/06513 (2013.01 - EP US); H01L 2225/06544 (2013.01 - EP US); H01L 2225/06589 (2013.01 - EP US); H01L 2924/15311 (2013.01 - EP US)

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